

Seat No : 3201 P R No : 201507401	Sex	c: M	Nan	ne: Bh	ASALE VINAY BHANUDAS
lo Of Attempts: 1		No Of	Gra	de	
		Credits	Obta	ned	SGPA
ASIC Design & FPGA					
	Theory	4	BB	Р	
	IA	2	AB	Р	
Digital Signal Processors & Embedded					
	Theory	4	BB	Р	
	IA	2	AB	Р	
Design for Testability & E-Waste Manage				_	
	Theory	4	ВС	Р	
	IA	2	AB	Р	
Processor Architecture & Parallel Proce	_				
	Theory	4	CC	Р	
	IA	2	BB	Р	
Memory Design		de-			
	Theory	4	BB	Р	
	IA	2	AA	Р	
Parallel Processing Lab					
1	IA	2	AB	P	
	Practical	2	BC	P	
FPGA & Embedded Systems Lab					
			A D		
	IA	2	AB	Р	
	Practical	2	AA	P	
					7.11 P
D.D.N. 2000	Practical Total :	38	AA	Р	PASSES
	Practical Total :	2 38	AA	Р	7.11 P PASSES DRKAR NEEL RAMAKANT
	Practical Total :	2 38 c: M No Of	AA Nam Gra	P ne: B0	PASSES DRKAR NEEL RAMAKANT
No Of Attempts : •1	Practical Total :	2 38	AA	P ne: B0	PASSES
	Practical Total:	2 38 C: M No Of Credits	Nam Gra Obta	P ne: B0 de ined	PASSES DRKAR NEEL RAMAKANT
lo Of Attempts : •1	Practical Total: Sex	2 38 C: M No Of Credits	Nam Gra Obta	P BC de ined	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA	Practical Total: Sex Theory	2 38 C: M No Of Credits	Nam Gra Obta	P ne: B0 de ined	PASSES DRKAR NEEL RAMAKANT
No Of Attempts : •1	Practical Total: Sex Theory IA Systems	2 38 C: M No Of Credits 4 2	Nam Gra Obta AA AA	P ne: B0 de ined P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA	Practical Total: Sex Theory IA Systems Theory	2 38 C: M No Of Credits 4 2	Nam Gra Obta AA AA	P me: B0 de ined P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded	Practical Total: Sex Theory IA Systems Theory IA	2 38 C: M No Of Credits 4 2	Nam Gra Obta AA AA	P ne: B0 de ined P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA	Practical Total: Sex Theory IA Systems Theory IA gement	2 38 C: M No Of Credits 4 2	Nam Gra Obta AA AA BB	P ne: BC de ined P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded	Practical Total: Sex Theory IA Systems Theory IA gement Theory	2 38 C: M No Of Credits 4 2 4 2	Nam Gra Obta AA AA BB AB	P ne: BC de ined P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Management	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA	2 38 C: M No Of Credits 4 2	Nam Gra Obta AA AA BB	P ne: BC de ined P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing	2 38 No Of Credits 4 2 4 2	Nam Gra Obta AA AA BB AB AB	P de: B0 de ined P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Management	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory	2 38 No Of Credits 4 2 4 2	Nam Gra Obta AA AA BB AB AB	P De: B0 de ined P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proces	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing	2 38 No Of Credits 4 2 4 2	Nam Gra Obta AA AA BB AB AB	P de: B0 de ined P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Management	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA	2 38 No Of Credits 4 2 4 2 4 2	Nam Gra Obta AA AA BB AB AB AB BC BB	P de: B0 de ined P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proces	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory	2 38 No Of Credits 4 2 4 2 4 2	Nam Gra Obta AA AA BB AB AB AB	P de: B0 de inned P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proce	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA	2 38 No Of Credits 4 2 4 2 4 2	Nam Gra Obta AA AA BB AB AB AB BC BB	P de: B0 de ined P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proces	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	2 38 C: M No Of Credits 4 2 4 2 4 2	Nam Gra Obta AA AB AB AB AB AC BC BB AB AA	P de: B0 de nned P P P P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proce	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA	2 38 C: M No Of Credits 4 2 4 2 4 2 4 2	Nam Gra Obta AA AB	P de: B0 de nned P P P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proce Memory Design Parallel Processing Lab	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	2 38 C: M No Of Credits 4 2 4 2 4 2	Nam Gra Obta AA AB AB AB AB AC BC BB AB AA	P de: B0 de nned P P P P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proce Memory Design	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA Practical	2 38 C: M No Of Credits 4 2 4 2 4 2 4 2	Nam Gra Obta AA AB AB AB AB AO BC BB AB AB AB AB AB AB BC BB BB	P de: B0 de ned P P P P P P P P P P P	PASSES DRKAR NEEL RAMAKANT
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proce Memory Design Parallel Processing Lab	Practical Total: Sex Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA	2 38 C: M No Of Credits 4 2 4 2 4 2 4 2	Nam Gra Obta AA AB	P de: B0 de nned P P P P P P P	PASSES DRKAR NEEL RAMAKANT

38

Total:

7.84 P PASSES



P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



COLLEGE: GOA COLLEGE OF ENGINEERING

No: 3203 PR No: 201108381	Se	x: F	Nam	ie:	GOVEKAR DIVYA DIGAMBAR
f Attempts: 1		No Of Credits	Grad		SGPA
ASIC Design & FPGA					
	Theory	4	BC	P	
	IA	2	BC	Р	
Digital Signal Processors & Embedded				-	
	Theory	4	CC	P	
Design for Tostobility & F Wests Manage	IA	2	CC	P	
Design for Testability & E-Waste Manag		4	00	В	
	Theory IA	4	CC BC	P	
Processor Architecture & Parallel Proces			ВС	P	
Processor Architecture & Paraller Proces	Theory	4	FF	F	
	IA	2	CC	Р	
Memory Design	1/4				
Memory Design	Theory	4	CC	Р	
	IA	2	ВС	Р	
Parallel Processing Lab		-	50		
and the second second	IA	2	ВС	Р	
1 Sec. 19	Practical	2	CC	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	Р	
	Practical	2	AB	P	
	Total:	38			5.11 F
	Total:	38			5.11 F FAILS
No: 3204 PRNo: 201006305	-	38 _. x: F	Nam	ie:	
No: 3204 PRNo: 201006305 f Attempts: 1	-	x: F No Of	Grad	de	FAILS
	-	x: F		de	FAILS KALSHAONKAR REEMA DATTARAM
f Attempts: 1	-	x: F No Of	Grad	de	FAILS KALSHAONKAR REEMA DATTARAM
f Attempts: 1	Se	x: F No Of Credits	Grad Obtai	de ned	FAILS KALSHAONKAR REEMA DATTARAM
Attempts: 1	Se:	x: F No Of Credits	Grad Obtai	de ned P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA	Theory IA Systems Theory	x: F No Of Credits	Grad Obtai	de ned P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S	Theory IA Systems Theory IA	No Of Credits	Grad Obtai AA AA	de ned P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA	Theory IA Systems Theory IA ement	No Of Credits 4 2 4 2	Grad Obtain AA AA BB AA	de ned P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S	Theory IA Systems Theory IA ement Theory	No Of Credits 4 2 4 2	Grad Obtain AA AA BB AA	de ned P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag	Theory IA Systems Theory IA ement Theory IA	No Of Credits 4 2 4 2	Grad Obtain AA AA BB AA	de ned P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S	Theory IA Systems Theory IA ement Theory IA ssing	No Of Credits 4 2 4 2	Grad Obtain AA AA BB AA AA AA	de ned P P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag	Theory IA Systems Theory IA ement Theory IA ssing Theory	No Of Credits 4 2 4 2 4 2	Grad Obtain AA AA AA AA AA	de ned P P P P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA Systems Theory IA ement Theory IA ssing	No Of Credits 4 2 4 2	Grad Obtain AA AA BB AA AA AA	de ned P P P P	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag	Theory IA Systems Theory IA ement Theory IA ssing Theory IA	No Of Credits 4 2 4 2 4 2	Grad Obtain AA AA AA AA AB AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory	No Of Credits 4 2 4 2 4 2 4 2	Grac Obtai AA AA AA AA AB AB AA	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Process Memory Design	Theory IA Systems Theory IA ement Theory IA ssing Theory IA	No Of Credits 4 2 4 2 4 2	Grad Obtain AA AA AA AA AB AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	AA AA AA AB AB AA AA	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Process Memory Design	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2 4 2	Grad Obtain AA AA AA AA AB AA AA AA	PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	AA AA AA AB AB AA AA	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Process Memory Design	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA IA Practical	No Of Credits 4 2 4 2 4 2 4 2 4 2	Grad Obtain AA AA AA AA AB AA AA AA AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA IA Practical	X: F No Of Credits 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4	Grad Obtain AA AA AB AA AB AA AA AB AB	de ned PP	FAILS KALSHAONKAR REEMA DATTARAM
ASIC Design & FPGA Digital Signal Processors & Embedded S Design for Testability & E-Waste Manag Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA IA Practical	No Of Credits 4 2 4 2 4 2 4 2 4 2	Grad Obtain AA AA AA AA AB AA AA AA AB	de ned PP	FAILS KALSHAONKAR REEMA DATTARAM



COLLEGE: GOA COLLEGE OF ENGINEERING

Seat No: 3205 P R No: 200907827	Se	x: F	Nam	ne :	KHANDEPARKAR SHWETA MAHENDRA
No Of Attempts: 1		No Of Credits	Gra		SGPA
ASIC Design & FPGA					
	Theory	4	AA	Р	
	IA	2	AA	Р	
Digital Signal Processors & Embedded				_	
	Theory	4	AB	P	
Decision for Trade little 0 F 10/2 to 10	IA	2	AA	P	
Design for Testability & E-Waste Manage			DD	_	
	Theory	4	BB	Р	
Processor Architecture & Parallel Proce	IA	2	AA	Р	
Processor Architecture & Parallel Proce		4	Λ Λ	-	
	Theory IA	2	AA AB	P	
Memory Design	IA	2	AD	P	
Memory Design	Theory	4	AB	Р	
	IA	2	AO	P	
Parallel Processing Lab	1/1	_	70		
. drailer i recessing Lab	IA	2	AA	Р	
	Practical	2	BB	Р	
FPGA & Embedded Systems Lab	radioai	_	00		
TT GAT a Emboaded Systems Lab	IA	2	AA	Р	
	Practical	2	AA	P	
	· raotioai	_	, , ,		
	Total:	38	THE REAL PROPERTY OF THE PERSONS	ON SHED MADE CO.	8 47 P
	Total:	38		000000000000000000000000000000000000000	8.47 P PASSES
Seat No : 3206 P R No : 201008499	100 EWODEROO FUORE BODE SCORFIDOR FOOR EFFORE FOOR	38 x: F	Nam	ne :	
Seat No : 3206 P R No : 201008499 No Of Attempts : 1	100 EWODEROO FUORE BODE SCORFIDOR FOOR EFFORE FOOR	x: F			PASSES KHARANGATE LAXIMI SHASHANK
No Of Attempts: 1	100 EWODEROO FUORE BODE SCORFIDOR FOOR EFFORE FOOR	1034F045D04FV04FV04FV04FV02FV02FV02FV0	Nam Grad Obtai	de	PASSES
	Sex	x: F No Of Credits	Grad Obtai	de ined	PASSES KHARANGATE LAXIMI SHASHANK
lo Of Attempts: 1	Sex	No Of Credits	Grad Obtai	de ined P	PASSES KHARANGATE LAXIMI SHASHANK
lo Of Attempts: 1 ASIC Design & FPGA	Sex Theory IA	x: F No Of Credits	Grad Obtai	de ined	PASSES KHARANGATE LAXIMI SHASHANK
o Of Attempts: 1	Sex Theory IA Systems	No Of Credits 4 2	Grad Obtai AA AA	de ined P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA	Theory IA Systems Theory	No Of Credits 4 2	Grad Obtain AA AA AB	de ined P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA Systems Theory IA	No Of Credits 4 2	Grad Obtai AA AA	de ined P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA	Theory IA Systems Theory IA gement	No Of Credits 4 2 4 2	Gradobtai AA AA AB AA	de ined P P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA Systems Theory IA gement Theory	No Of Credits 4 2 4 2	Gradobtai AA AA AB AA	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage	Theory IA Systems Theory IA gement Theory IA	No Of Credits 4 2 4 2	Gradobtai AA AA AB AA	de ined P P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA Systems Theory IA gement Theory IA sessing	No Of Credits 4 2 4 2	Grad Obtain AA AA AB AA AB	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage	Theory IA Systems Theory IA gement Theory IA essing Theory	No Of Credits 4 2 4 2 4 2	Grad Obtain AA AB AA AB AB BB	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces	Theory IA Systems Theory IA gement Theory IA sessing	No Of Credits 4 2 4 2	Grad Obtain AA AA AB AA AB	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage	Theory IA Systems Theory IA gement Theory IA essing Theory IA	No Of Credits 4 2 4 2 4 2	AA AA AB AA AB AB AB	P P P P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage	Theory IA Systems Theory IA gement Theory IA sssing Theory IA Theory	No Of Credits 4 2 4 2 4 2 4 2	AA AA AB AA AB AB AB	PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design	Theory IA Systems Theory IA gement Theory IA essing Theory IA	No Of Credits 4 2 4 2 4 2	AA AA AB AA AB AB AB	P P P P P	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	AA AA AB AA AB AB AB AA AA	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2 4 2	AA AA AB AA AB AB AB AA AA	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	AA AA AB AA AB AB AB AA AA	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA Practical	No Of Credits 4 2 4 2 4 2 4 2 4 2	AA AA AB AB AB AB AA AA AA AA BB	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA IA Practical	X: F No Of Credits 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4	AA AB AB AB AA AA AA BB AA	de ined PP	PASSES KHARANGATE LAXIMI SHASHANK
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Manage Processor Architecture & Parallel Proces Memory Design Parallel Processing Lab	Theory IA Systems Theory IA gement Theory IA essing Theory IA Theory IA IA Practical	No Of Credits 4 2 4 2 4 2 4 2 4 2	AA AA AB AB AB AB AA AA AA AA BB	de ined PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	PASSES KHARANGATE LAXIMI SHASHANK







COLLEGE: GOA COLLEGE OF ENGINEERING Seat No: 3207 PRNo: 201105539 Name: KORDE CHARUDATTA GURUDAS Sex: M No Of Attempts: 1 Grade No Of **SGPA** Credits Obtained ASIC Design & FPGA Theory 4 AB P IA 2 P AA Digital Signal Processors & Embedded Systems Theory 4 BB P 2 AB P Design for Testability & E-Waste Management 4 BC P Theory IA 2 AB P Processor Architecture & Parallel Processing 4 CC P Theory 2 P IA AA Memory Design Theory 4 AB P IA 2 AA P Parallel Processing Lab IA 2 AA P Practical 2 AB P FPGA & Embedded Systems Lab IA 2 AA P Practical 2 AB P Total: 38 7.63 P PASSES PRNo: 201107707 Name: MAHATME MOHIT BHAIRAV Seat No: 3208 Sex: M No Of Attempts: 1 No Of Grade SGPA Credits Obtained ASIC Design & FPGA P 4 BB Theory P IA 2 BB Digital Signal Processors & Embedded Systems Theory 4 BC P P IA 2 CC Design for Testability & E-Waste Management P Theory 4 BC P IA 2 AB Processor Architecture & Parallel Processing CC P Theory 4 P IA 2 BB Memory Design BC P Theory 4 P IA 2 AA Parallel Processing Lab 2 AB P IA Practical 2 AB P FPGA & Embedded Systems Lab 2 AB P IA Practical 2 AB P 6.74 P PASSES Total: 38

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



eat No: 3209 PR No: 20100735	Se:	x: F	Nam	e: MA	YEKAR MITH	IILI NARAYAN	
o Of Attempts: 1		No Of Credits	Gra		SGPA		
ASIC Design & FPGA							
	Theory	4	BB	P			
	IA	2	AB	P			
Digital Signal Processors & Embedde	d Systems						
	Theory	4	BB	P			
	IA	2	CC	P			
Design for Testability & E-Waste Mana							
	Theory	4	BB	P			
	IA	2	CC	Р			
Processor Architecture & Parallel Proc				_ * * * *			
	Theory	4	CC	P			
	IA	2	CC	Р			
Memory Design	T1.	7	-				
	Theory	4	CC	Р			
Develled Decease in the	IA	2	AB	Р			
Parallel Processing Lab	1.6	2		р			
	IA Danation	2	BB	Р			
EDCA & Embodded Systems Lab	Practical	2	CC	Р			
FPGA & Embedded Systems Lab	IA	2	DD	В			
	Practical	2	BB	P P			
	Practical	2	BB	P			
			*******************************	· · · · · · · · · · · · · · · · · · ·		***************************************	TENNS DESCRIPTION OF THE PROPERTY OF THE PROPE
	Total:	38	***************************************	or opening construction and production	6.26 P	Result Reserve	
eat No : 3210 P.R.No : 20100630	•		Nam	e NA	***************************************	Sem I Not Pass	ed
eat No : 3210 PR No : 201006306	•	x: F			***************************************		ed
eat No : 3210 P R No : 201006306 o Of Attempts : 1	•	x: F No Of	Gra	de	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1	•	x: F		de	***************************************	Sem I Not Pass	ed
	3 Se	x: F No Of Credits	Grad Obtai	de	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1	•	x: F No Of	Gra	de ned	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA	3 Se:	x: F No Of Credits	Grad Obtai	de ned P	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1	3 Se:	x: F No Of Credits	Grad Obtai	de ned P	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA	Theory IA	No Of Credits	Grad Obtain BB AA	de ned P	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA	Theory IA d Systems Theory IA	No Of Credits 4 2	Grad Obtain BB AA BC	de ned P P	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1 ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA d Systems Theory IA	No Of Credits 4 2	Grad Obtain BB AA BC	de ned P P	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1 ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA Systems Theory IA agement	No Of Credits 4 2 4 2	Gradobtai BB AA BC BB	de ned P P P	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana	Theory IA I Systems Theory IA agement Theory IA	x: F No Of Credits 4 2 4 2	BB AA BC BB	de ned P P P	IK STHRIGDI	Sem I Not Pass	ed
Of Attempts: 1 ASIC Design & FPGA Digital Signal Processors & Embedded	Theory IA I Systems Theory IA agement Theory IA	x: F No Of Credits 4 2 4 2	BB AA BC BB	de ned P P P	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana	Theory IA I Systems Theory IA Igement Theory IA cessing	No Of Credits 4 2 4 2	BB AA BC BB BC	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana	Theory IA I Systems Theory IA agement Theory IA ressing Theory	No Of Credits 4 2 4 2 4 2	BB AA BC BB BC	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Processor	Theory IA I Systems Theory IA agement Theory IA ressing Theory	No Of Credits 4 2 4 2 4 2	BB AA BC BB BC	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Processor	Theory IA I Systems Theory IA Igement Theory IA Igessing Theory IA	No Of Credits 4 2 4 2 4 2	BB AA BC BB BC FF BB	de ned P P P P P P P P P P P P P P P P P P P	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Processor	Theory IA I Systems Theory IA I Germany IA I Heory IA I Theory IA I Theory IA I Theory IA I Theory IA	No Of Credits 4 2 4 2 4 2 4 2	BB AA BC BB BC FF BB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proc Memory Design	Theory IA I Systems Theory IA I Germany IA I Heory IA I Theory IA Theory IA Theory	No Of Credits 4 2 4 2 4 2 4 2	BB AA BC BB BC FF BB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proc Memory Design	Theory IA d Systems Theory IA agement Theory IA dessing Theory IA Theory IA	No Of Credits 4 2 4 2 4 2 4 2	BB AA BC BB BC FF BB AA AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proc Memory Design	Theory IA d Systems Theory IA agement Theory IA dessing Theory IA Theory IA IA	No Of Credits 4 2 4 2 4 2 4 2 4 2	BB AA BC BB BC FF BB AA AB AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proc Memory Design Parallel Processing Lab	Theory IA d Systems Theory IA agement Theory IA dessing Theory IA Theory IA IA	No Of Credits 4 2 4 2 4 2 4 2 4 2	BB AA BC BB BC FF BB AA AB AB	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed
ASIC Design & FPGA Digital Signal Processors & Embedded Design for Testability & E-Waste Mana Processor Architecture & Parallel Proc Memory Design Parallel Processing Lab	Theory IA I Systems Theory IA I Sessing Theory IA I Heory IA Theory IA Theory IA Theory IA Theory IA Theory IA	X: F No Of Credits 4 2 4 2 4 2 4 2 4 2	BB AA AB AB CC	de ned PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP	IK STHRIGDI	Sem I Not Pass	ed



KIL

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



Seat No: 3211 PR No: 201008518	Se	x: F	Nam	ne: NAI	K TEJA UDAY	,
No Of Attempts: 1		No Of Credits	Gra		SGPA	
ASIC Design & FPGA		Orcans	Obtu	ilica		
	Theory	4	AB	P		
	IA	2	AA	Р		
Digital Signal Processors & Embedded S	Systems					
	Theory	4	BC	P		
	IA	2	BC	P		
Design for Testability & E-Waste Manag	ement					
	Theory	4	BB	P		
	IA	2	BC	P		
Processor Architecture & Parallel Proces	ssing					
	Theory	4	CC	P		
	IA	2	BB	P		
Memory Design						
	Theory	4	AB	Р		
	IA	2	AB	Р		
Parallel Processing Lab						
	IA	2	BB	P		
	Practical	2	CC	P		
FPGA & Embedded Systems Lab						
	IA	2	BB	P		
	Practical	2	BB	P		
	Total:	38			6.84 P	
					PASSES	
Seat No: 3212 P R No: 201107719	Se	x: M	Nam	ne: PAT	TIL ABHIJEET	VILAS
No Of Attempts: 1		No Of	Gra	de		
		Credits	Obta	ned	SGPA	
ASIC Design & FPGA	_			_		
	Theory	4	BB	Р		
	IA	2	BB	Р		
Digital Signal Processors & Embedded S	-					
	Theory	4	ВС	P		
	IA	2	CC	Р		
Design for Testability & E-Waste Manage				_		
	Theory	4	ВС	Р		
	IA	2	BC	Р		
Processor Architecture & Parallel Proces				_		
	Theory	4	FF	F		
N. D. D. L.	IA	2	BB	Р		
Memory Design	_			_		
	Theory	4	ВС	Р		
Developed Developed	IA	2	BB	Р		
Parallel Processing Lab						
	IA .	2	BB	Р		
FD0.4.0.F	Practical	2	CC	Р		
FPGA & Embedded Systems Lab						
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		2	A D	P		
	IA	2	AB			
	Practical Total:	2 38	AB	P	5.79 F	Result Reserve

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average



Seat No : 3213 P R No : 201105565	Sex	c: M	Nam	ne:	RANE KARAN PARSHURAM
lo Of Attempts: 1		No Of Credits	Gra		SGPA
ASIC Design & FPGA		Orodito	Obta	nou	
	Theory	4	AB	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded	Systems				
	Theory	4	BB	P	
	IA	2	AA	P	
Design for Testability & E-Waste Manag	ement				
	Theory	4	AB	P	
	IA	2	AO	P	
Processor Architecture & Parallel Proce					
	Theory	4	ВС	P	
	IA	2	AB	Р	
Memory Design			, , ,		
, – – – – – – – – – – – – – – – – – – –	Theory	4	ВВ	Р	
	IA	2	AA	Р	
Parallel Processing Lab	I/A	2	^^		
araner i rocessing Lab	IA	2	AA	Р	
	Practical	2	AA	Р	
EDCA & Embadded Systems Lab	Fractical	2	AA	-	
FPGA & Embedded Systems Lab	1.0	2	^ ^	D	
	IA Danatia al	2	AA	Р	
	Practical	2	AA	Р	
	Total:	38			8.05 P
2t No. 2044 D.D.N. 004400240	0		N.L.		PASSES
Seat No : 3214 P R No : 201106312	Sex	: M	Nam	ie:	SAWAL SAGAR NAMDEV
lo Of Attempts: 1		No Of	Grad		SGPA
ASIC Decign & EDCA		Credits	Obtai	ned	SGFA
ASIC Design & FPGA					
		4	AD		
	Theory	4	AB	Р	
Digital Cinnal Days are a Section 11 at 1	IA	2	AB BB	P P	
Digital Signal Processors & Embedded	IA Systems	2	BB	Р	
Digital Signal Processors & Embedded	IA Systems Theory	2	BB	P P	
	IA Systems Theory IA	2	BB	Р	
Digital Signal Processors & Embedded State Design for Testability & E-Waste Manag	IA Systems Theory IA ement	4 2	BB BB CC	P P	
	IA Systems Theory IA ement Theory	2 4 2	BB	P P	
Design for Testability & E-Waste Manag	IA Systems Theory IA ement Theory IA	4 2	BB BB CC	P P	
	IA Systems Theory IA ement Theory IA sssing	2 4 2	BB CC BB BB	P P P P	
Design for Testability & E-Waste Manag	IA Systems Theory IA ement Theory IA sssing Theory	2 4 2	BB CC BB BB	P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proce	IA Systems Theory IA ement Theory IA sssing	2 4 2 4 2	BB CC BB BB	P P P P	
Design for Testability & E-Waste Manag	IA Systems Theory IA ement Theory IA sssing Theory	2 4 2 4 2	BB CC BB BB	P P P P	
Design for Testability & E-Waste Manage	IA Systems Theory IA ement Theory IA sssing Theory	2 4 2 4 2	BB CC BB BB	P P P P	
Design for Testability & E-Waste Manage Processor Architecture & Parallel Proce	IA Systems Theory IA ement Theory IA ssing Theory IA	2 4 2 4 2	BB CC BB BB AB	P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proce	IA Systems Theory IA ement Theory IA ssing Theory IA Theory	2 4 2 4 2 4 2	BB BB CC BB BB AB AB BB	P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proce Memory Design	IA Systems Theory IA ement Theory IA ssing Theory IA Theory	2 4 2 4 2 4 2	BB BB CC BB BB AB AB BB	P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proce Memory Design	IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA	2 4 2 4 2 4 2	BB BB CC BB BB AB AB AB AA	P P P P P P	
Processor Architecture & Parallel Proce Memory Design Parallel Processing Lab	IA Systems Theory IA ement Theory IA ssing Theory IA Theory IA	2 4 2 4 2 4 2	BB CC BB BB AB AB	P P P P P P P	
Design for Testability & E-Waste Manag Processor Architecture & Parallel Proce Memory Design	IA Systems Theory IA ement Theory IA sssing Theory IA Theory IA IA Practical	2 4 2 4 2 4 2 2 2	BB BB CC BB BB AB AB AB AB BB	P P P P P P P P P P P P P P P P P P P	
Design for Testability & E-Waste Manage Processor Architecture & Parallel Proce Memory Design Parallel Processing Lab	IA Systems Theory IA ement Theory IA sssing Theory IA Theory IA IA Practical	2 4 2 4 2 4 2 2 2 2	BB BB CC BB BB AB AB AB AA BB AA BB AA BB	P P P P P P P P P	
Design for Testability & E-Waste Manage Processor Architecture & Parallel Proce Memory Design Parallel Processing Lab	IA Systems Theory IA ement Theory IA sssing Theory IA Theory IA IA Practical	2 4 2 4 2 4 2 2 2	BB BB CC BB BB AB AB AB AB BB	P P P P P P P P P P P P P P P P P P P	7.42 P

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COLLEGE: GOA COLLEGE OF ENGINEERING

	Total:	38	ВС		3.89 F	Result Reserve Sem I Not Passed
	Practical	2	BC	P		
FPGA & Embedded Systems Lab	IA	2	СС	Р		
FDOA A Foot added Outland Lab	Practical	2	BC	Р		
	IA	2	BB	Р		
Parallel Processing Lab						
	IA	2	CC	P		
	Theory	4	FF	F		
Memory Design						
	IA	2	BC	P		
	Theory	4	FF	F		
Processor Architecture & Parallel Pro	cessing					
	IA	2	CC	Р		
	Theory	4	FF	F		
Design for Testability & E-Waste Mar	nagement					
	IA	2	CC	Р		
	Theory	4	CC	Р		
Digital Signal Processors & Embedde						
	IA	2	BB	P		
ASIC Design & FFGA	Theory	4	ВС	Р		
ASIC Design & FPGA		Credits	Obta	ined	SGPA	
No Of Attempts: 1		No Of	Gra		SGPA	
Seat No : 3215 PR No : 2010073	34 36	ex: M	IVall	ie. Sn	ETGAONKAR	ANAY ANIL

Seat No: 3216 P R No: 200801358	Se	x: F	Nam	me : PARKER NEHA PRASAD	
No Of Attempts : 2 ASIC Design & FPGA		No Of Credits	Grad Obtai	0004	
Acid Besign at 1 GA	Theory	4	AA	P	
	IA	2	AA	+	
Digital Signal Processors & Embedded S		- 0000	, , ,		
3	Theory	4	BC	P	
	IA	2	ВВ	+	
Design for Testability & E-Waste Manag	ement				
	Theory	4	AB	P	
	IA	2	AA	+	
Processor Architecture & Parallel Proces	ssing				
	Theory	4	FF	F	
	IA	2	BB	+	
Memory Design					
	Theory	4	AB	P	
	IA	2	AA	+	
Parallel Processing Lab					
	IA	2	BC	+	
	Practical	2	BC	+	
FPGA & Embedded Systems Lab					
	IA	2	AB	+	
	Practical	2	AB	+	
	Total:	38		6.89 F	

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
ВВ	. 7	Good
ВС	6	Fair
CC	5	Satisfactory
FF	0	Fail

Checked By : KPL

10/8/2016 S.S.J. Figueiredo Assistant Registrar-E(Proff.)

Registrar

Controller Of Examinations

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average