GOA UNIVERSITY
Taleigao Plateau, Goa 403 206

REVALUATION RESULT REGISTER FOR M.E ELECTRONICS & TELECOMMUNICATION (MICROELECTRONICS) SEMESTER - II
EXAMINATION HELD IN MAY 2016 Course : Revised Course - 2013

1803
14/10/16

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3203 P R No : 201108381 Sex : F Name : GOVEKAR DIVYA DIGAMBAR
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA				
	Theory	4	BC P	
	IA	2	BC P	
Digital Signal Processors & Embedded Systems				
	Theory	4	CC P	
	IA	2	CC P	
Design for Testability & E-Waste Management				
	Theory	4	CC P	
	IA	2	BC P	
Processor Architecture & Parallel Processing				
	Theory	4	FF F	
	IA	2	CC P	
Memory Design				
	Theory	4	CC P	
	IA	2	BC P	
Parallel Processing Lab				
	IA	2	BC P	
	Practical	2	CC P	
FPGA & Embedded Systems Lab				
	IA	2	AB P	
	Practical	2	AB P	
	Total : NO CHANGE	38		5.11 F FAILS

Seat No : 3208 P R No : 201107707 Sex : M Name : MAHATME MOHIT BHAIRAV
No Of Attempts : 1

		No Of Credits	Grade Obtained	SGPA
ASIC Design & FPGA				
	Theory	4	BB P	
	IA	2	BB P	
Digital Signal Processors & Embedded Systems				
	Theory	4	BC P	
	IA	2	CC P	
Design for Testability & E-Waste Management				
	Theory	4	BC P	
	IA	2	AB P	
Processor Architecture & Parallel Processing				
	Theory	4	CC P	
	IA	2	BB P	
Memory Design				
	Theory	4	BC P	
	IA	2	AA P	
Parallel Processing Lab				
	IA	2	AB P	
	Practical	2	AB P	
FPGA & Embedded Systems Lab				
	IA	2	AB P	
	Practical	2	AB P	
	Total : NO CHANGE	38		6.74 P PASSES

Acad

NB|WB|HEIC

536
14/10/16

P: Passes; F: Fails; A/ABS: Absent; N/NAP: Non Appearance; X/NE: Not Eligible; +: Grades Carried Over; SGPA: Semester Grade Point Average; CGPA: Cummulative Grade Point Average

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Course : Revised Course - 2013

COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3210 P R No : 201006308 Sex : F Name : NAIK STHRIGDHARA NAVANATH
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	BB	P	
	IA	2	AA	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	BB	P	
	IA	2	BB	P	
Design for Testability & E-Waste Management					
	Theory	4	AB	P	
	IA	2	BC	P	
Processor Architecture & Parallel Processing					
	Theory	4	FF	F	
	IA	2	BB	P	
Memory Design					
	Theory	4	AA	P	
	IA	2	AB	P	
Parallel Processing Lab					
	IA	2	AB	P	
	Practical	2	CC	P	
FPGA & Embedded Systems Lab					
	IA	2	BB	P	
	Practical	2	BB	P	
	Total :	38			6.63 F FAILS

Seat No : 3212 P R No : 201107719 Sex : M Name : PATIL ABHIJEET VILAS
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	BB	P	
	IA	2	BB	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	BC	P	
	IA	2	CC	P	
Design for Testability & E-Waste Management					
	Theory	4	BC	P	
	IA	2	BC	P	
Processor Architecture & Parallel Processing					
	Theory	4	FF	F	
	IA	2	BB	P	
Memory Design					
	Theory	4	BC	P	
	IA	2	BB	P	
Parallel Processing Lab					
	IA	2	BB	P	
	Practical	2	CC	P	
FPGA & Embedded Systems Lab					
	IA	2	AB	P	
	Practical	2	AB	P	
	Total :	38			5.79 F Result Reserve
	NO CHANGE				Sem I Not Passed

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COLLEGE : GOA COLLEGE OF ENGINEERING

Seat No : 3215 P R No : 201007394 Sex : M Name : SHETGAONKAR ANAY ANIL
No Of Attempts : 1

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	BC	P	
	IA	2	BB	P	
Digital Signal Processors & Embedded Systems					
	Theory	4	CC	P	
	IA	2	CC	P	
Design for Testability & E-Waste Management					
	Theory	4	FF	F	
	IA	2	CC	P	
Processor Architecture & Parallel Processing					
	Theory	4	FF	F	
	IA	2	BC	P	
Memory Design					
	Theory	4	CC	P	
	IA	2	CC	P	
Parallel Processing Lab					
	IA	2	BB	P	
	Practical	2	BC	P	
FPGA & Embedded Systems Lab					
	IA	2	CC	P	
	Practical	2	BC	P	
	Total :	38			4.42 F FAILS

Seat No : 3216 P R No : 200801358 Sex : F Name : PARKER NEHA PRASAD
No Of Attempts : 2

		No Of Credits	Grade Obtained		SGPA
ASIC Design & FPGA					
	Theory	4	AA	P	
	IA	2	AA	+	
Digital Signal Processors & Embedded Systems					
	Theory	4	BC	P	
	IA	2	BB	+	
Design for Testability & E-Waste Management					
	Theory	4	AB	P	
	IA	2	AA	+	
Processor Architecture & Parallel Processing					
	Theory	4	FF	F	
	IA	2	BB	+	
Memory Design					
	Theory	4	AA	P	
	IA	2	AA	+	
Parallel Processing Lab					
	IA	2	BC	+	
	Practical	2	BC	+	
FPGA & Embedded Systems Lab					
	IA	2	AB	+	
	Practical	2	AB	+	
	Total :	38			7.00 F FAILS

GOA UNIVERSITY TALEIGAO PLATEAU GOA

Grade	Grade Points	Performance
AO	10	Outstanding
AA	9	Excellent
AB	8	Very Good
BB	7	Good
BC	6	Fair
CC	5	Satisfactory
FF	0	Fail

Read By :
Checked By : 12/10/16
Date : 13/10/16

12/10/2016
S.S.J. Figueiredo
Assistant Registrar-E(Proff.)

12/10/16
Leo V. Macedo
Controller Of Examinations

13/10/16
M. Shreedhara
Offg. Registrar

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