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**S.E. (Electronics & TC / Electronics & Comm Engg) (Sem-III)**  
**(Revised Course 2016-2017) EXAMINATION NOV/DEC 2019**  
**Digital System Design**

[Duration : Three Hours]

[Total Marks : 100]

**Instructions:**

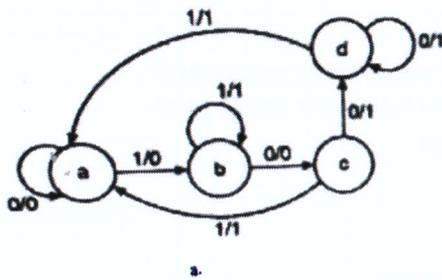
- 1) Assume suitable data, if necessary.
- 2) All symbols and abbreviations carry their usual meaning.
- 3) Answer any 5 questions by selecting **two questions from Part-A, two questions from Part-B and one question from Part-C.**

**PART A**

1.
  - a) Given that  $(211)_x = (152)_8$  find the value of base X. 3
  - b) Express the decimal number '9865' in 10
    - a) BCD
    - b) EXCESS-3
    - c) Binary
    - d) Octal
    - e) Hexadecimal
  - c) Subtract  $(25)_{10} - (34)_{10}$  using ones complement method. 4
  - d) Add  $(-88.75)_{10}$  to  $(-36.25)_{10}$  using two's complement method. 3
2.
  - a) Simplify the expression using K-Maps method. 4  
 $F = \sum m(0,2,6,10,11,12,13) + d(3,4,5,14,15)$ . Implement using NAND-Logic only.
  - b) Implement the following Boolean function with 8:1 multiplexer 4  
 $F(A, B, C, D) = \pi M(0,3,5,8,9,10,12,14)$
  - c) Prove that  $(A + B)((AC)' + C)(B' + AC)' = A'B$  3
  - d) Simplify the following equation and find out the minterms for the following equation. 3  
 $f(A, B, C, D) = (AB' + A'B)(C + C'D)$
  - e) Design a 4-bit binary to Gray Code Converter. 6
3.
  - a) Design and explain how a BCD ADDER using IC74LS83 can be used to add BCD numbers. Draw the logic diagram. 7
  - b) Write the characteristics table, excitation table and equation of a clocked JK flip flop. Draw the logic diagram of a clocked JK flip flop. Convert JK F/F to a T F/F. 7
  - c) Design an Octal to Binary encoder circuit. 6

**PART B**

4. a) A sequential network has one input and one output. The state diagram is shown below. Design the sequential circuit using T-flipflops. 8



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- b) A binary ripple counter is required to count upto  $(16383)_{10}$  in terms of decimal. How many flip-flops are required? If the clock frequency  $f_{in}$  is 8.19MHz, what is the output frequency. 8
- c) Design a modulo-5 ripple counter using the J-K Flip-Flop. Draw the timing diagram for the same. 8

5. a) Answer the following questions w.r.t counters: 10
- i) What do you mean by 'Lockout' in synchronous counters? How the problem of lockout is eliminated?
  - ii) Design a MOD-6 asynchronous counter using T-FF. Draw the timing diagram.
  - iii) What are the disadvantages of ripple counters?
- b) With the help of a diagram, explain the working of a Wallace tree multiplier. 6
- c) Draw the timing sequence for the 4-bit Johnson counter and explain. 4

6. a) Design a type T synchronous counter that goes through the states 0,3,5,6,0.... Is the counter Self-Starting? 7
- b) Define the following points w.r.t Digital IC's: 8
- 1) Fan-in
  - 2) Fanout
  - 3) Propagation delay
  - 4) Noise margin
- c) Draw and explain Totem-pole TTL3 input NAND gate. Why Totem-pole TTL cannot be used for wire AND operation? 5

**PART C**

7. a) Draw and explain the CMOS to TTL interfacing. 6
- b) What is race around condition? How can it be overcome? 6
- c) With the help of a neat diagram explain the working of Universal Shift Register. 8
8. a) Reduce the following expression in SOP & POS. 7
- $$f = \sum (0,2,3,10,11,12,13,16,17,18,19,20,21,26,27)$$
- b) Design 16:1 Mux using 8:1 Mux. 6
- c) What are the characteristics of ECL digital logic family. Draw neat diagram of ECL logic gate and explain its operation. 7