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S.E. (Electronics & TC/Electronics & Comm Engg) (Semester- III)
(Revised Course 2007-08) EXAMINATION Nov/Dec 2019
Digital System Design

[Duration : Three Hours]

[Total Marks : 100]

Instruction

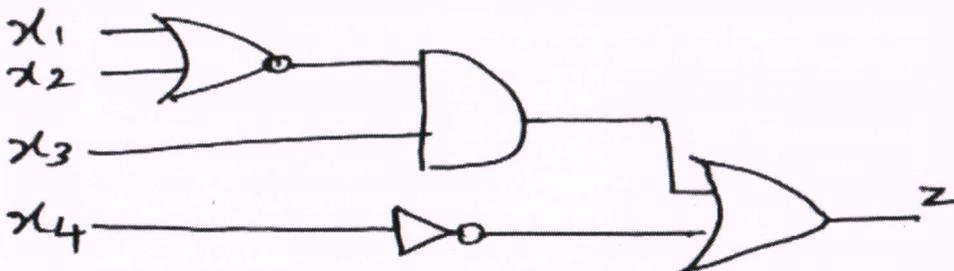
- 1) Answer *five* questions in full with at least *one* question from *each* Module.
- 2) Missing data, if any, may be suitably assumed.

Module- 1

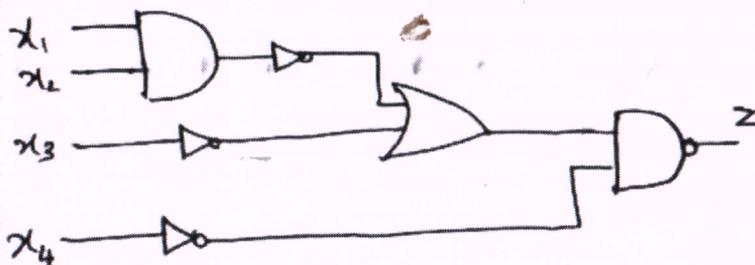
Q.1 a) Simplify the expression using K map method and draw the logic diagram. **05**

$$F = \sum m [0, 1, 4, 5, 6, 8, 9, 12, 13, 14]$$

b) Simplify the logic diagram and implement the expression with NAND gates only. **05**



c) Convert the following AOI logic circuit to NOR logic. **05**



d) Show how EX-OR can be used as a controlled Inverter? **05**

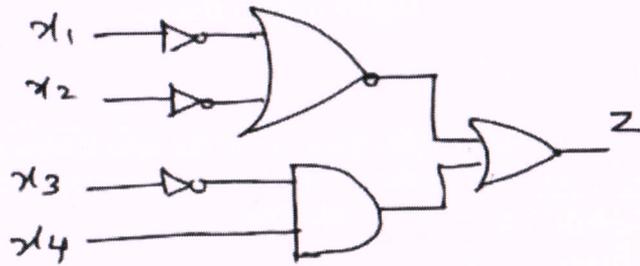
Q.2 a) Answer the following questions: **14**

- i. Show how NOR logic gates can be used to implement Ex-NOR logic.
- ii. Given that $(211)_x = (152)_8$, Find the value of base x.
- iii. Add the numbers $(AB)_{16} + (BF)_{16}$ and convert the sum to decimal.
- iv. Write the truth table for NOR gate
- v. Can an EX-NOR gate act as an Inverter? Explain.
- vi. Add the following binary numbers a) $[10011101]$ & b) $[11101101]$ and convert the result to Gray code.

vii. Write the canonical POS form for $Y = A + \bar{B}C$

b) Redraw the circuit given below after simplification

06



Module- 2

Q.3

- a. (i) Design a Half- Adder circuit using only two input NAND gates. (6)
- (ii) Reuse the Half Adder circuit to design a FULL ADDER circuit.
- b. Implement the following Boolean Function with a 8:1 Multiplexer where, $F(A, B, C, D) = \sum m (0, 2, 6, 10, 15) + d (3, 9, 13)$ (6)
- c. Write the characteristic table and equation of a Clocked D flip- flop. Draw the logic diagram of a Clocked D flip- Flop using NAND gates. Also find the output Q in the following waveforms? Clear and Preset are the active low asynchronous inputs of the D FF. (8)

Q.4

- a. What is 'RACE AROUND CONDITION' in Flip-Flops? How can this be overcome? (6)
- b. Write the Characteristic table and equation of a Clocked JK flip-flop. Draw the Logic diagram of a clocked JK flip-flop using NAND gates. (8)
- c. How will you convert TFF to a JK FF? (6)

Module- 3

Q.5

- a) With reference to the Asynchronous counter, What is meant by the 'Modulus of the Counter'? (8)
 - (i) How are SYNCHRONOUS and ASYNCHRONOUS counters different from each other?
 - (ii) Draw a 2 bit Asynchronous UP counter using negative edged JK Flip Flop.
- b) compare with logic diagram and timing sequences: 4 bit basic Ring and Johnson counter using D flip Flops. How will the logic change if JK flip flops are used? (8)
- c) Compare SIPO and PIPO shift registers. (4)

- Q.6 a) Design a MOD-4 Asynchronous down counter using T flip- flops. How will the design differ for a MOD 4 Synchronous Down counter using T flip flops? (10)
- b) Design a synchronous counter using JK Flip Flops that goes through states 3, 4, 6, 7, 3 (10)
- Draw the State Diagram
 - Draw and design the logic diagram for the above counter using JK Flip Flops.

Module- 4

- Q.7 1. Explain the following: (15)
- Integrated Injection Logic NAND gate.
 - Characteristic of ECL digital Logic Family
 - Working of the CMOS Inverter

2. Draw and explain the working of a CMOS NAND gate using transistors. How is it Different form the TTL NAND gate? Explain (5)

- Q.8 1. Draw and explain the CMOS to TTL interfacing (8)
2. For a static RAM memory of size **1K x 8** (8)

- The Memory chip has two active low control signals, Chip select (CS) and WE (write enable).
- The RAM memory contains the following 8 bit data, (F0)₁₆ in the first memory location and (AA)₁₆ in the last memory location.

Also, a Microprocessor, has 16 bit unidirectional address lines, 8 bit bidirectional data bus and Read/ Write control signal among others signals.

- How many data and address lines does the memory chip (1K X 8) have?
- If a memory of size **4K x 8** is to be interfaced with the Microprocessor ,how many (**1K x 8**) memory chips are required?
- Write the memory address ranges for this 4K x 8 memory and draw the arrangement.

3. Implement the following Boolean Equation in CMOS logic: (4)
- $F = \overline{A + B}$
 - $F = \overline{A \cdot B}$