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S.E. (Electrical & Electronics) (Semester- III) (Revised Course 2007-08)
 EXAMINATION NOV/DEC 2019
 Digital Integrated Circuits

[Duration : Three Hours]

[Total Marks : 100]

Instructions:

1. Answer **any 5** questions in full, with atleast **One** question from **each** Module.
2. Missing data, if any may be suitably assumed.

MODULE-I

- Q.1**
- a) Perform following Conversion. 8
 - i) $(163.875)_{10}$ to Binary
 - ii) $(11011.101)_2$ to Decimal
 - iii) $(9EAF2)_{16}$ to Octal
 - iv) $(756.603)_8$ to Hexadecimal
 - b) Perform following operation using two's complement method. 4
 - i) $(64)_{10} + (-28)_{10}$
 - ii) $(35)_{10} + (-28)_{10}$
 - c) Reduce the following using Quin-Mc Cluskey Method. 8
 - i) $F = \sum(0,1,2,8,10,11,14,15)$
- Q.2**
- a) Simplify the following using Boolean Algebra. 6
 - i) $F=A(B+C'((AB)'+(AC')))$
 - ii) $F=(B+BC).(B+B'C).(B+D)$
 - b) Discuss Error detection and Error correction codes. 5
 - c) Implement the function $F=W.X.Y+X.Y.Z+Y.Z.W$ using NAND gates. 6
 - d) Represent the decimal Number 8620 in BCD and Excess 3 Code. 3

MODULE-II

- Q.3**
- a) Design a Full adder using Half adder, draw a neat logic diagram and explain the design with a truth table. 7
 - b) What is a magnitude comparator? Discuss the 4-bit magnitude comparator. 6
 - c) Implement the following function using a suitable multiplexer. 7
 Draw a neat connection diagram
- $$F(A, B, C, D) = \sum(1,3,4,11,12,13,14,15)$$
- Q.4**
- a) Design BCD to seven segment decoder. 8
 - b) Design the logic diagram of a 4-bit priority Encoder. Design the truth table and explain the logic. 6
 - c) Design 1×4 Demultiplexer using logic gates and explain its working. 6

MODULE-III

- Q.5**
- a) Implement the following Boolean function with a PLA. 8
 - i) $F1(A,B,C)=\sum(0,1,2,4)$
 - ii) $F2(A, B, C) = \sum(0,5,6,7)$
 - b) Explain with timing diagram the various modes of operation of a DRAM. 8
 - c) Differentiate between PLA and PAL. 4
- Q.6**
- a) Explain the following memories 8
 - i) SRAM ii) PROM iii) EPROM iv) FLASH
 - b) With a neat Diagram explain the logic construction of a 32×4 ROM. Discuss the importance of ROM. 8
 - c) Compare between RAM and ROM. 4

MODULE-IV

- Q.7**
- a) Draw the logic diagram of a SR flip flop and write its truth table, excitation table. 6
 - b) Explain the working of MOD-5 counter. 6
 - c) Explain the 4-bit parallel in serial out shift register with a neat logic diagram and timing waveform. 8
- Q.8**
- a) With respect to a flip flop, discuss the following timings. 8
 - i) Set up time
 - ii) Hold time
 - iii) Clock skew
 - b) Differentiate between Synchronous and Asynchronous counter. Draw the timing waveform for a 4-bit synchronous and Asynchronous counter. 12